IME00-015

1. A radio frequency (RF) electrostatic discharge (ESD) protection circuit for integrated circuits (IC) with a plurality of power supplies, comprising:

on a substrate, a dual-mode shunt system providing a low impedance path for ESD, said dual-mode shunt system further comprising

a pair of power supply rails consisting of a first and a second power supply rail;

a power supply in communication with said first and said second power supply rail;

a transient-type power shunt circuit in communication with said first and said second power supply rail, said power shunt circuit comprising at least an RC timer circuit and a CMOS inverter driver, said power shunt circuit providing a low impedance path for an ESD between said first and said second power supply rail, said power shunt circuit designed to turn on when the voltage ramp on said first power supply rail is faster than a RC time-constant, intrinsic to said power shunt circuit, and larger than the threshold voltage (Vt) of a PMOS transistor;

a dual-diode scheme, comprising a serially coupled first and second I/O diode, formed in-between said first and said second power supply rail, the junction of said first and said second I/O diode coupled to an I/O pad, said first and said second I/O diode providing a conductive path for said ESD, said dual diode scheme ensuring that the capacitance at said I/O pad is bias independent for RF signal inputs; and

a plurality of said dual-mode shunt systems, each supplied by its own power supply operable at any supply voltage, said plurality of said dual-mode shunt systems all coupled together via said second power supply rail, said plurality of said dual-mode shunt systems capable of operating at any voltage of said power supplies, said first power supplies isolated from each other.

2. The circuit of claim 1, wherein said plurality of said dual-mode shunt systems is coupled together via said second power supply rails, each of said second power supply rails coupled to another second power supply rail by means of a set of complementary polarity diodes, said complementary polarity diodes isolating said plurality of second power supply rails from each other, to limit power supply noise cross talk.

3. The circuit of claim 2, wherein the voltage between any of said plurality of second power supplies does not differ by more than one diode drop.

4. The circuit of claim 1, wherein said power shunt circuit is in close proximity to said one or more I/O pads by providing one of said power shunt circuits per said pair of power supply rails.

5. The circuit of claim 1, wherein said complementary polarity diodes are P+/N-well diodes made in an N-well/P-substrate process.

6. The circuit of claim 5, wherein said complementary polarity diodes are N+/P-substrate diodes when said second power supply rail is coupled to said substrate of said IC.

7. The circuit of claim 1, wherein additional I/O pads are coupled via additional first and second I/O diodes to said first and said second power supply rail.

8. The circuit of claim 1, wherein said power shunt circuit, in one preferred embodiment, comprises:

said RC timer circuit , to provide said RC time-constant, further comprising:

a first, a second, and a third PMOS transistor coupled in series, the source of said first PMOS transistor coupled to said first power supply rail, the drain of said third PMOS transistor coupled to a node A, the gates of said first, said second, and said third PMOS transistor coupled to said second power supply rail, said first, said second, and said third PMOS transistor acting as a resistive means, thereby creating a large resistance in a small area;

a fourth PMOS transistor having its source and drain coupled to said second power supply rail and having its drain coupled to said node A, said fourth PMOS transistor wired to function as a capacitive means, said resistive means together with said fourth PMOS transistor acting as said RC time-constant;

said CMOS inverter driver, formed by a fifth PMOS transistor and a first NMOS transistor coupled in series, such that the source of said fifth PMOS transistor is coupled to said first power supply rail and the source of said first NMOS transistor is coupled to said second power supply rail, the junction of said fifth PMOS transistor and said first NMOS transistor coupled to a node D, and the gate of said fifth PMOS transistor and said first NMOS transistor coupled to said node A, said CMOS inverter driver providing drive current; and

a second NMOS transistor, its drain and source coupled between said first and said second power supply rail, respectively, and the gate of said second NMOS transistor coupled to said node D, said second NMOS transistor shunting an ESD from said first power supply rail to said second power supply rail.

9. The circuit of claim 8, wherein said CMOS inverter driver has its trip point skewed high to speed the turn-on of said second NMOS transistor by selecting a width ratio between said fifth PMOS transistor and said second NMOS transistor of about 4:1, respectively.

10. The circuit of claim 8, wherein said second NMOS transistor has a width/length dimension of about 2000/0.35 microns, respectively.

11. The circuit of claim 8, wherein said fourth PMOS transistor by operating in the accumulation region provides a large capacitance in the range from 0 Volt to the threshold voltage Vt.

12. The circuit of claim 8, wherein said power shunt circuit, in another preferred embodiment, further comprises:

a first inverter coupled between said first and said second power supply rail, said first inverter improving the turn-on speed of said power shunt circuit, the input of said first inverter coupled to said node A, the output of said first inverter labeled node B, said first inverter providing a normal mid-swing point;

a second inverter coupled between said first and said second power supply rail, said second inverter improving the turn-on speed of said power shunt circuit, the input of said second inverter coupled to said node B, the output of said second inverter labeled node C, the input response of said second inverter skewed to preferentially keep said node C low during an ESD event;

a sixth PMOS transistor having its source and drain coupled to said second power supply rail and having its drain coupled to said node C, said sixth PMOS transistor thus wired to function as a capacitive means, said sixth PMOS transistor together with said fifth PMOS transistor acting as a capacitive voltage divider;

said gate of said CMOS inverter driver coupled to said node C; and

an increase in the width of said second NMOS transistor to about 6000 micron, said second NMOS transistor thereby clamping said first rail to a much lower voltage.

13. The circuit of claim 12, wherein said sixth PMOS transistor by operating in the accumulation region provides a large capacitance in the range from 0 Volt to the threshold voltage Vt.

14. The circuit of claim 12, wherein said mid-swing point of said first inverter insures when no ESD event is present, that noise on said first power supply rail will not turn on said power shunt circuit for longer than an RC time-constant formed by a resistive component of said second inverter and the total capacitance at node C.

15. The circuit of claim 12, wherein said sixth PMOS transistor, acting as a capacitive means, holds low node C when a voltage spike occurs at said first power supply rail, thus diminishing a bootstrap effect caused by a drain-to-gate capacitance of said fifth PMOS transistor.

16. The circuit of claim 1, wherein the cathode of said first I/O diode is coupled to said first power supply, and the anode of said first I/O diode is coupled to said I/O pad, said first I/O diode arranged as a P+ diffusion/N-well diode thusly:

where the anode and the cathode of said first I/O diode correspond to said P+ diffusion and said N-well, respectively;

where said P+ diffusion of said first I/O diode is arranged in a rectangular shape, the area of said rectangular shape determined by the number of contacts needed to pass a target current;

where said P+ diffusion further comprises an array of said contacts;

where an N-well tap of width **S** surrounds said P+ diffusion on all four sides; and

where contacts for each of said I/O pads further surround on all four sides said N-well tap, said contacts arranged on each side in one or more rows.

17. The circuit of claim 16, wherein said dimension **S** is set to a minimum to produce the lowest parasitic resistance in said N-well taps.

18. The circuit of claim 16, wherein said rectangular area for said P+ diffusion has sides of equal length to achieve the largest perimeter/area ratio for the largest current/capacitance ratio.

19. The circuit of claim 16, wherein the capacitance of said first I/O diode is less than 200 femtoF (femtoF=10^{-15} Farad)

20. The circuit of claim 16, wherein a plurality of said first I/O diodes are arranged in a two-dimensional array.

21. The circuit of claim 1, wherein the anode of said second I/O diode is coupled to said second power supply, and the cathode of said second I/O diode is coupled to said I/O pad, said second I/O diode arranged as an N+ diffusion/P-substrate diode thusly:

where the cathode and the anode of said second I/O diode correspond to said N+ diffusion and said P-substrate, respectively;

where said N+ diffusion of said second I/O diode is arranged in a rectangular shape, the area of said rectangular shape determined by the number of contacts needed to pass a target current;

where said N+ diffusion further comprises an array of said contacts;

where a P-substrate tap of width **S** surrounds said N+ diffusion on all four sides; and

where contacts for each of said I/O pads further surround on all four sides said P-substrate tap, said contacts arranged on each side in one or more rows.

22. The circuit of claim 21, wherein said dimension **S** is set to a minimum to produce the lowest parasitic resistance in said P-substrate taps.

23. The circuit of claim 21, wherein said rectangular area for said N+ diffusion has sides of equal length to achieve the largest perimeter/area ratio for the largest current/capacitance ratio.

24. The circuit of claim 21, wherein the capacitance of said second I/O diode is less than 200 femtoF (femtoF=10^{-15} Farad)

25. The circuit of claim 21, wherein a plurality of said second I/O diodes are arranged in a two-dimensional array.

26. A radio frequency (RF) electrostatic discharge (ESD) protection circuit for integrated circuits (IC) with a plurality of power supplies, comprising:

on a substrate, a dual-mode shunt system providing a low impedance path for ESD, said dual-mode shunt system further comprising

a pair of power supply rails consisting of a first and a second power supply rail;

a power supply in communication with said first and said second power supply rail;

a transient-type power shunt circuit in communication with said first and said second power supply rail, said power shunt circuit comprising timer and driver circuits, said power shunt circuit providing a low impedance path for an ESD between said first and said second power supply rail, said power shunt circuit designed to turn on when the voltage ramp on said first power supply rail is faster than a RC time-constant, intrinsic to said power shunt circuit, and larger than the threshold voltage (Vt) of a PMOS transistor;

a first and a second I/O diode formed in-between said first and said second power supply rail, the junction of said first and said second I/O diode coupled to an I/O pad, said first and said second I/O diode providing a conductive path for said ESD; and

a plurality of said dual-mode shunt systems, each supplied by its own power supply operable at any supply voltage, said plurality of said dual-mode shunt systems all coupled together via said second power supply rail, said plurality of said dual-mode shunt systems capable of operating at any voltage of said power supplies, said first power supplies isolated from each other.

27. The circuit of claim 26, wherein said plurality of said dual-mode shunt systems is coupled together via said second power supply rails, each of said second power supply rails coupled to another second power supply rail by means of a set of complementary polarity diodes, said complementary polarity diodes isolating said plurality of second power supply rails from each other, to limit power supply noise cross talk.

28. The circuit of claim 27, wherein the voltage between any of said plurality of second power supplies does not differ by more than one diode drop.

29. The circuit of claim 26, wherein said power shunt circuit is in close proximity to said one or more I/O pads by providing one of said power shunt circuits per said pair of power supply rails.

30. The circuit of claim 26, wherein said complementary polarity diodes are P+/N-well diodes made in an N-well/P-substrate process.

31. The circuit of claim 30, wherein said complementary polarity diodes are N+/P-substrate diodes when said second power supply rail is coupled to said substrate of said IC.

32. The circuit of claim 26, wherein additional I/O pads are coupled via additional first and second I/O diodes to said first and said second power supply rail.

33. The circuit of claim 26, wherein said power shunt circuit comprises said timer circuit in communication with said driver circuit, said timer and driver circuits utilizing metal oxide semiconductor (MOS) switching devices coupled between said first and said second power supply rail.

34. The circuit of claim 26, wherein the cathode of said first I/O diode is coupled to said first power supply, and the anode of said first I/O diode is coupled to said I/O pad, said first I/O diode arranged as a P+ diffusion/N-well diode thusly:

where the anode and the cathode of said first I/O diode correspond to said P+ diffusion and said N-well, respectively;

where said P+ diffusion of said first I/O diode is arranged in a rectangular shape, the area of said rectangular shape determined by the number of contacts needed to pass a target current;

where said P+ diffusion further comprises an array of said contacts;

where an N-well tap of width **S** surrounds said P+ diffusion on all four sides; and

where contacts for each of said I/O pads further surround on all four sides said N-well tap, said contacts arranged on each side in one or more rows.

35. The circuit of claim 26, wherein the anode of said second I/O diode is coupled to said second power supply, and the cathode of said second I/O diode is coupled to said I/O pad, said second I/O diode arranged as an N+ diffusion/P-substrate diode thusly:

where the cathode and the anode of said second I/O diode correspond to said N+ diffusion and said P-substrate, respectively;

where said N+ diffusion of said second I/O diode is arranged in a rectangular shape, the area of said rectangular shape determined by the number of contacts needed to pass a target current;

where said N+ diffusion further comprises an array of said contacts;

where a P-substrate tap of width **S** surrounds said N+ diffusion on all four sides; and

where contacts for each of said I/O pads further surround on all four sides said P-substrate tap, said contacts arranged on each side in one or more rows.